Silicon Gate MOS 2107A

FULLY DECODED RANDOM ACCESS 4096 BIT DYNAMIC MEMORY

* **Access Time -- 300 ns max.**
* **Refresh Period -- 2 ms**

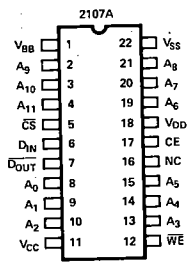
- **Low Cost Per Bit**
- **Low Standby Power**
- **Easy System Interface**
- **Only One High Voltage Input Signal—Chip Enable**
- **Low Level Address, Data, Write Enable, Chip Select Inputs**
- **Address Registers Incorporated on the Chip**
- **Simple Memory Expansion—Chip Select Input Lead**
- **Fully Decoded—On Chip Address Decode**
- **Output is Three State and TTL Compatible**
- **Ceramic and Plastic 22-Pin DIPs**

The Intel 2107A is a 4096 word by 1 bit dynamic n-channel MOS RAM. It was designed for memory applications where very low cost and large bit storage are important design objectives. The 2107A uses dynamic circuitry which reduces the operation and standby power dissipation.

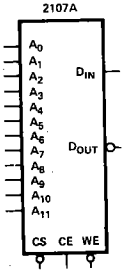
Reading information from the memory is non-destructive. Refreshing is accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic one or a logic zero.

The 2107A is fabricated with n-channel silicon gate technology. This technology allows the design and production of high performance, easy to use MOS circuits and provides a higher functional density on a monolithic chip than other MOS technologies.

PIN CONFIGURATION



LOGIC SYMBOL

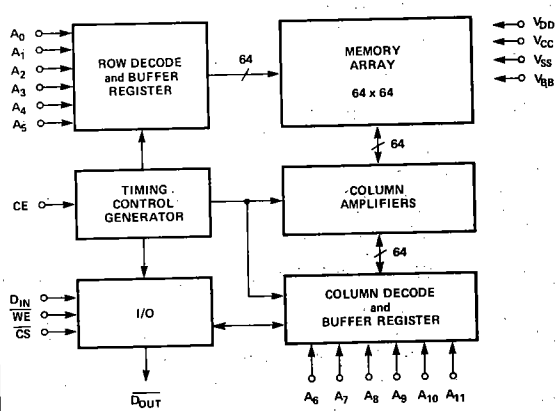


PIN NAMES

D_{IN}	DATA INPUT	CE	CHIP ENABLE
A_0-A_{11}	ADDRESS INPUTS*	$\overline{D_{OUT}}$	DATA OUTPUT
$\overline{WE}$	WRITE ENABLE	V_{CC}	POWER (+5V)
$\overline{CS}$	CHIP SELECT	NC	NOT CONNECTED

*Refresh Addresses A_0-A_5.

BLOCK DIAGRAM



Absolute Maximum Ratings*

Temperature Under Bias ..... 0°C to 70°C

Storage Temperature ..... −65°C to +150°C

All Input or Output Voltages with Respect to the most Negative Supply Voltage, V_{BB} ..... +25V to −0.3V

Supply Voltages V_{DD}, V_{CC}, and V_{SS} with Respect to V_{BB} ..... +20V to −0.3V

Power Dissipation 1.0W

**COMMENT:*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} [1] = -5V ± 5%, V_{SS} = 0V, unless otherwise notes.

Symbol	Parameter	Limits			Unit	Conditions
		Min.	Typ.[2]	Max.		
I_{LI}	Input Load Current (all inputs except CE)		.01	10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
I_{LC}	Input Load Current		.01	10	μA	V_{IN} = $V_{IL\ MIN}$ to $V_{IH\ MAX}$
$\|I_{LO}\|$	Output Leakage Current for high impedance state		.01	10	μA	CE = -1V to +.8V or $\overline{CS}$ = 3.5V, V_O = 0V to 5.25V
I_{DD1}	V_{DD} Supply Current during CE off[3]		.1	100	μA	CE = -1V to +.8V
I_{DD2}	V_{DD} Supply Current during CE on		14	22	mA	CE = V_{IHC}, T_A = 25°C
$I_{DD\ AV}$	Average V_{DD} Supply Current		23	34	mA	Cycle time = 700ns, t_{CEW} = 480ns, T_A = 25°C, Fig. 1,3
I_{CC1}	V_{CC} Supply Current during CE off		.01	10	μA	CE = -1V to +.8V
I_{CC2}	V_{CC} Supply Current during CE on		5	10	mA	CE = V_{IHC}, T_A = 25°C
$I_{CC\ AV}$	Average V_{CC} Supply Current		6	10	mA	Cycle time = 700ns, t_{CEW} = 480ns T_A = 25°C, Fig. 2,4
I_{BB}	V_{BB} Supply Current		1	100	μA	
V_{IL}	Input Low Voltage[4]	−1.0		0.8	V	
V_{IH}	Input High Voltage[4]	3.5		V_{CC} +1	V	
V_{ILC}	CE Input Low Voltage[4]	−1.0		+1.0	V	
V_{IHC}	CE Input High Voltage	V_{DD} −1		V_{DD} +1	V	
V_{OL}	Output Low Voltage[4]	0.0		0.45	V	I_{OL} = 1.7mA, Fig. 6
V_{OH}	Output High Voltage[4]	2.4		V_{CC}	V	I_{OH} = -100μA, Fig. 5

NOTES:

1. The only requirement for the sequence of applying voltage to the device is that V_{DD}, V_{CC}, and V_{SS} should never be .3V or more negative than V_{BB}.
2. Typical values are for T_A = 25°C and nominal power supply voltages.
3. The I_{DD} and I_{CC} currents flow to V_{SS}. The I_{BB} current is the sum of all leakage currents.
4. Referenced to V_{SS} unless otherwise noted.

D.C. Characteristics

Fig. 1. I_{DD} AVERAGE VS. TEMPERATURE

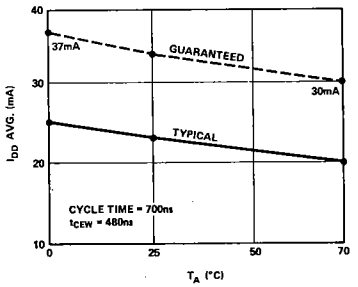


Fig. 2. I_{CC} AVERAGE VS. TEMPERATURE

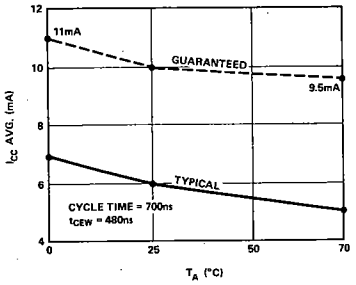


Fig. 3. TYPICAL I_{DD} AVERAGE VS. CYCLE TIME

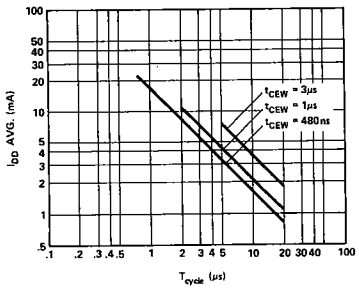


Fig. 4. TYPICAL I_{CC} AVERAGE VS. CYCLE TIME

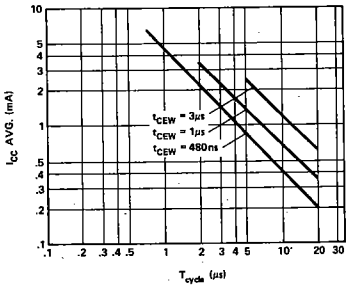


Fig. 5. TYPICAL I_{OH} VS. V_{OH}

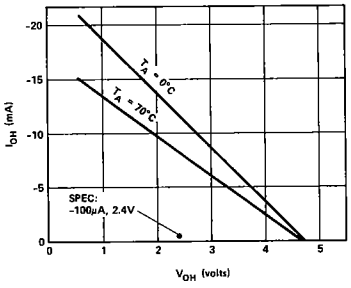


Fig. 6. TYPICAL I_{OL} VS. V_{OL}

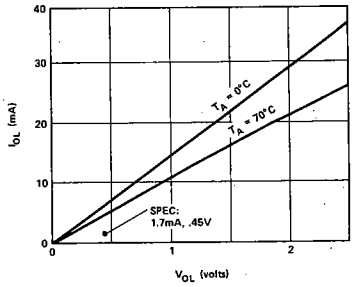


Fig. 7. TYPICAL REFRESH VS. TEMPERATURE

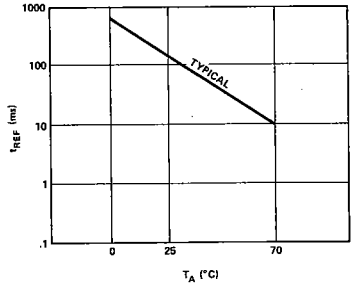
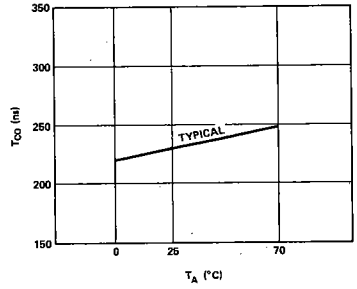


Fig. 8. TYPICAL ACCESS TIME VS. TEMPERATURE



RAMs

A.C. Characteristics $T_A = 0°C$ to $70°C$, $V_{DD} = 12V \pm 5\%$, $V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$,

READ, WRITE, AND READ MODIFY/WRITE CYCLE $V_{SS} = 0V$, unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{REF}	Time Between Refresh		2	ms	
t_{AC}	Address to CE Set Up Time	0		ns	
t_{AH}	Address Hold Time	100		ns	
t_{CC}	CE Off Time	180		ns	
t_T	CE Transition Time		50	ns	
t_{CF}	CE Off to Output High Impedance State	0		ns	

READ CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RCY}	Read Cycle Time	500		ns	$t_T = 20ns$
t_{CER}	CE On Time During Read	280	3000	ns	
t_{CO}	CE Output Delay		280	ns	$C_{load} = 50pF$, Load = One TTL Gate,
t_{ACC}	Address to Output Access		300	ns	Ref = 2.0V for High, 0.8V for Low.
t_{WL}	CE to $\overline{WE}$ Low	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$
t_{WC}	$\overline{WE}$ to CE on	0		ns	

WRITE CYCLE

Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{WCY}	Write Cycle Time	700		ns	$t_T = 20ns$
t_{CEW}	CE Width During Write	480	3000	ns	
t_W	$\overline{WE}$ to CE Off	340		ns	
t_{CW}	CE to $\overline{WE}$ High	300		ns	
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{CD} [1]	CE to D_{IN} Set Up		50	ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{WP}	$\overline{WE}$ Pulse Width	150		ns	
t_{WW}	$\overline{WE}$ Wait	0		ns	
t_{WC}	$\overline{WE}$ to CE On	0		ns	

Capacitance [2] $T_A = 25°C$

Symbol	Test	Plastic And Ceramic Pkg. Typ.	Max.	Unit	Conditions
C_{AD}	Address Capacitance, $\overline{CS}$, $\overline{WE}$, D_{IN}	3	6	pF	$V_{IN} = V_{SS}$
C_{CE}	CE Capacitance	17	25	pF	$V_{IN} = V_{SS}$
C_{OUT}	Data Output Capacitance	3	6	pF	$V_{OUT} = 0V$

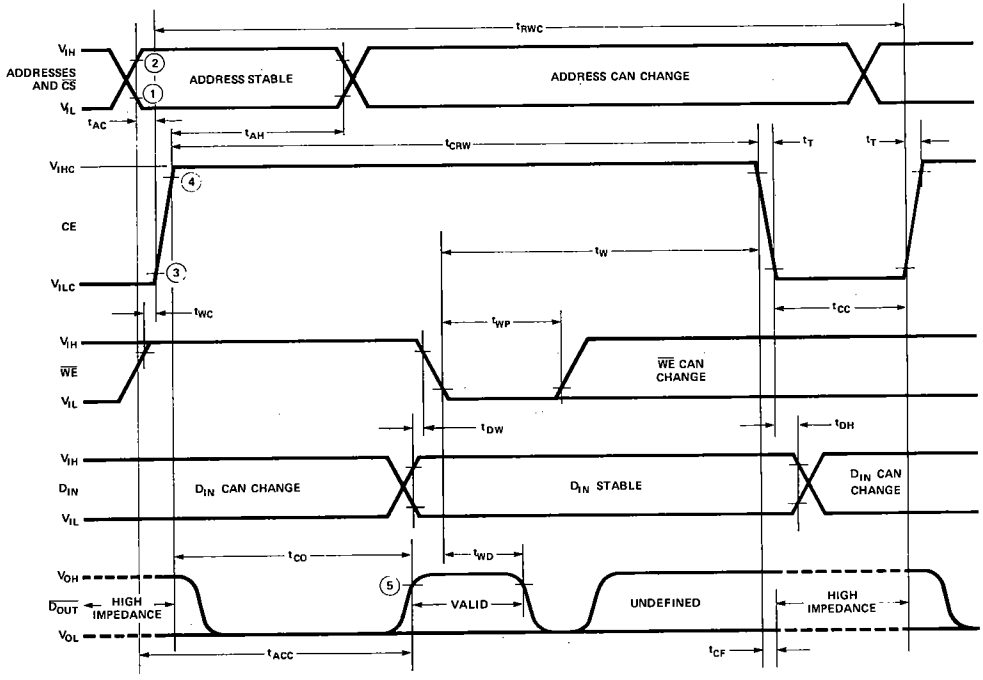
Notes: 1. t_{CD} applies only when $t_W > t_{CEW} - 50$ ns.

2. Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = \frac{I \Delta t}{\Delta V}$ with the current equal to a constant 20mA.

Read Modify Write Cycle

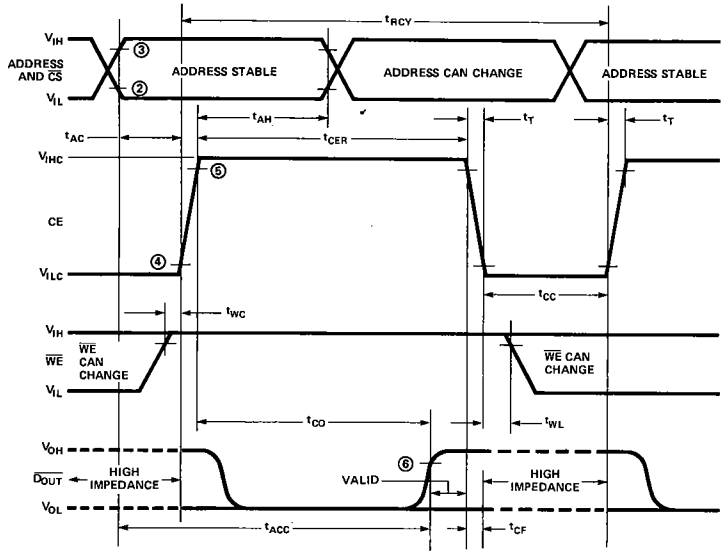
Symbol	Parameter	Min.	Max.	Unit	Conditions
t_{RWC}[1]	Read Modify Write(RMW) Cycle Time	840		ns	t_T = 20ns
t_{CRW}	CE Width During RMW	620	3000	ns	
t_{WC}	$\overline{WE}$ to CE on	0		ns	
t_W	$\overline{WE}$ to CE off	340		ns	C_{load} = 50pF, Load = One TTL Gate,
t_{WP}	$\overline{WE}$ Pulse Width	150		ns	Ref = 2.0V for High, 0.8V for Low.
t_{DW}	D_{IN} to $\overline{WE}$ Set Up	0		ns	
t_{DH}	D_{IN} Hold Time	0		ns	
t_{CO}	CE to Output Delay		280	ns	
t_{ACC}	Access Time		300	ns	
t_{WD}	$\overline{D_{OUT}}$ Valid After $\overline{WE}$	0		ns	$t_{ACC} = t_{AC} + t_{CO} + 1t_T$

Note 1. $t_{CRW} - t_W = t_{CO}$.

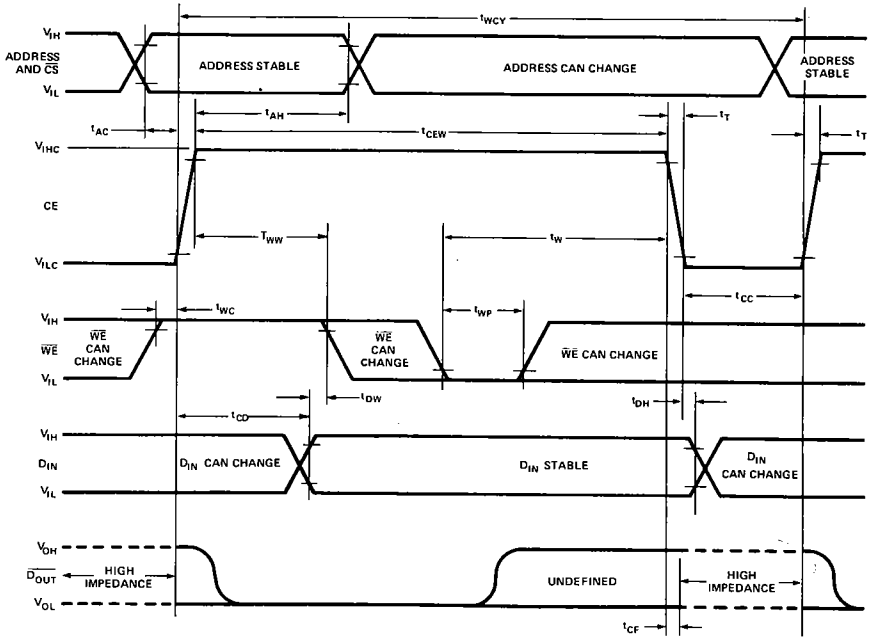


NOTES:
1. V_{SS} + 1.5V is the reference level for measuring timing of the address CS, WE, and D_{IN}.
2. V_{SS} + 3.0V is the reference level for measuring timing of the address, CS, WE, and D_{IN}.
3. V_{SS} + 2.0V is the reference level for measuring timing of CE.
4. V_{DD} -2V is the reference level for measuring timing of CE.
5. V_{SS} + 2.0V is the reference level for measuring the timing of D_{OUT}.

Read and Refresh Cycle [1]



Write Cycle



NOTES:
1. For Refresh cycle row and column addresses must be stable before t_{AC} and remain stable for entire t_{AH} period.
2. V_{SS} + 1.5V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
3. V_{SS} + 3.0V is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$, and D_{IN}.
4. V_{SS} + 2.0V is the reference level for measuring timing of CE.
5. V_{DD} -2V is the reference level for measuring timing of CE.
6. V_{SS} + 2.0V is the reference level for measuring the timing of $\overline{D_{OUT}}$.